MORNING SESSION

10 a.m. Welcome:
Bilal Akin – Associate Professor, UT Dallas

10:10 a.m. Keynote:
Arjang Hassibi – Founder and CEO, InSilixa, Inc.
Mass-deployable Molecular Diagnostics (MDx),
including COVID-19 Testing: An IC Designer Perspective
Q&A Moderated by Yiorgos Makris – Professor, UT Dallas

10:55 a.m. Student Research Interaction Poster Highlights:
Presented by Joseph Friedman – Assistant Professor, UT Dallas

11:25 a.m. Student Research Interaction Poster Session
Presented by Carlos Busso – Professor, UT Dallas

BREAK

12:30 p.m. – 1:30 p.m. CDT

AFTERNOON SESSION

1:30 p.m. Panel Session: IC Design in The Era of Deep Learning
Organized by Pavan Hanumolu – Professor, UIUC
Q&A Moderated by Naresh Shanbhag – Professor, UIUC

2:30 p.m. Center Overview:
Ken O – Director of TxACE, UT Dallas

2:45 p.m. Student Poster Awards:
Presented by Carlos Busso – Professor, UT Dallas
10 a.m. CDT

Welcome

BIO: Dr. Akin received a Ph.D. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2007. He was an R&D Engineer with Toshiba Industrial Division, Houston, TX, USA, from 2005 to 2008. From 2008 to 2012, he worked as an R&D Engineer at C2000 DSP Systems, Texas Instruments Incorporated. Since 2012, he has been with The University of Texas at Dallas as faculty. Dr. Akin is a recipient of the NSF CAREER ’15 award, IEEE IAS Transactions 1st Place Prize Paper Award, and Top Editors Recognition Award from IEEE TVT Society, Jonsson School Faculty Research Award, and Jonsson School Faculty Teaching Award. He is an Associate Editor of IEEE Transactions on Industry Applications and IEEE Transactions on Vehicular Technology. His research interests include design, control, and condition monitoring of power electronics components and systems, digital power control and management, fault diagnosis and condition monitoring of ac drives and motors.

Bilal Akin
Associate Professor
The University of Texas at Dallas

10:10 a.m. CDT

Mass-deployable Molecular Diagnostics (MDx), including COVID-19 Testing: An IC Designer Perspective

ABSTRACT: In the past year, the outbreak of COVID-19 has affected many lives globally. The suboptimal response to the pandemic revealed systematic deficiencies and gaps in our modern healthcare system. One specific area with consequential shortcomings was the diagnosis of infection and the pathogen, particularly the absence (or delayed deployment) of precision tests where was needed and when was needed. In this talk, we will take the opportunity to discuss and review highly customized IC technologies, broadly defined, that have the potential to address this unmet need, specifically integrated biosensors and CMOS biochip systems. First, we will review the system-level requirements of molecular diagnostics (MDx) systems and explain how they identify the unique DNA/RNA sequences of the pathogen (e.g., COVID-19 one-hour PCR test) to detect infections while achieving appropriate clinical specificity and selectivity. Next, we will discuss in detail methods by which we can design and implement MDx sensors using IC technologies. We will provide specific examples, tradeoff analysis, and manufacturing options for realizing a true CMOS MDx biochip. In the end, we will list key challenges and potential opportunities in this field.

BIO: Arjang Hassibi (S’99–M’05–SM’10) received the B.Sc. degree the highest honor from the University of Tehran in 1997, and the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University in 2001 and 2005, respectively. He had his post-doctoral training at the California Institute of Technology. He is currently the CEO of InSilixa Inc., a start-up company that he founded in 2012. Before that, he was a faculty member with the Electrical and Computer Engineering Department and the Institute for Cellular and Molecular Biology, The University of Texas at Austin. He also has held various research and development positions in industry and academia, including being a research scientist at the Stanford Genome Technology Center and the CMOS High-Speed Integrated Circuits (CHIC) Laboratory at Caltech; visiting professor at IBM Research at Yorktown; and co-founder and VP of engineering at Xagros Genomics. His areas of interest and expertise all include within the intersection of biotechnology and engineering, specifically biosensors and bioelectronics, biomedical electronics, and integrated sensors.
Panel: IC Design in The Era of Deep Learning

Panel Abstract: Deep learning (DL) has proven to be enormously successful in solving problems previously thought to be intractable in a diverse set of domains. This panel explores the potential and applicability of DL-based techniques in the integrated circuit (IC) design space. Specifically, the panel features experts from both industry and academe who will share their thoughts on questions such as: Will artificial intelligence and DL techniques lead to automation of analog and radio-frequency (RF) IC designs and make analog/RF designers obsolete? Or is it yet another over-hyped technology bound to fail as its predecessors have? Will DL approaches be effective in reducing design effort and increase productivity? Or will its hard-to-interpret outcomes and unpredictability make it an unsuitable tool? What role does DL play in electronic design automation and IC testing today and what are its future prospects? Finally, the panelists will discuss the impact of DL on career opportunities in the semiconductor area available to both undergraduate and graduate students.

Organizer
Pavan Hanumolu
Professor
University of Illinois, Urbana-Champaign

BIO: Pavan Hanumolu is a Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. His research interests are in the design of energy-efficient analog integrated circuits. Pavan is the Editor-in-Chief of the Journal of Solid-State Circuits and has served as a technical program committee member of the International Solid-State Circuits Conference, Custom Integrated Circuits Conference, and VLSI Circuits Symposium. He is an IEEE Fellow.

Moderator
Naresh Shanbhag
Professor
University of Illinois, Urbana-Champaign

BIO: Naresh R. Shanbhag is the Jack Kilby Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. His research focuses on the design of energy-efficient systems for machine learning, communications, and signal processing spanning algorithms, architectures and integrated circuits. Dr. Shanbhag received the 2018 SIA/SRC University Researcher Award, received the 2006 IEEE Solid-State Circuits Society’s Best Paper Award and served on the wireline subcommittee of International Solid-State Circuits Conference. In 2000, Dr. Shanbhag co-founded and served as the CTO of Intersymbol Communications, Inc. (now part of Finisar Corporation) which introduced mixed-signal ICs for electronic dispersion compensation of OC-192 optical links. From 2013-17, he was the founding Director of the Systems On Nanoscale Information fabriCs [SONIC] Center, a 5-year multi-university center funded by DARPA and SRC under the STARnet program. He has served on the wireline subcommittee of International Solid-State Circuits Conference. He is an IEEE Fellow.
Panelist: Tanay Karnik
Principal Engineer and Director of Heterogeneous Platforms Lab
Intel Labs

**BIO:** Tanay Karnik is a Principal Engineer and Director of the Heterogeneous Platforms Lab of Intel Labs. Previously he was the Director of Intel’s University Research Office. He received his Ph.D. in Computer Engineering from the University of Illinois at Urbana-Champaign and joined Intel Corporation in 1995. His research interests are in the areas of heterogeneous integration, small form factor systems, 3D architectures, variation tolerance, power delivery, and architectures for novel devices. He has published over 80 technical papers, has 92 issued, and 35 pending patents in these areas. He received an Intel Achievement Award for the pioneering work on integrated power delivery. He has served on 7 Ph.D. students’ committees. He is a member of ISSCC, DAC, ICCAD, IICDT, ISVLSI, ISCAS, 3DIC, and ISQED program committees and JSSC, TCAD, TVLSI, TCAS review committees. Tanay is General Chair of ISLPED’14, ASQED’10, ISQED’09, ISQED’08, and IICDT’08. Tanay is an IEEE Fellow, an ISQED Fellow, an Associate Editor for TVLSI, a Senior Advisory Board Member of JETCAS, and a Guest Editor for JSSC.

Panelist: Mahesh Mehendale
TI Fellow
Kilby Labs

**BIO:** Mahesh Mehendale is a TI Fellow and leads the Nano-power Foundational Technology at Kilby Labs. His current areas of focus include ultra-low power circuits and micro-architectures for “always-on” intelligent sensor nodes. Before this, he worked on architectures for low-power micro-controllers and high-definition (HD) video compression. Since joining TI in 1986, he has led the development of multiple industry-leading digital and system-on-chip (SoC) designs, including C27x/C28x DSPs and DM642 digital media processor. Mahesh has published more than 50 papers at international conferences/journals and presented many invited talks/tutorials. He has co-authored a book on “VLSI synthesis of DSP kernels” and two book chapters. Mahesh holds 19 U.S. patents and was elected senior member of IEEE in 2000. He received the “Distinguished Alumnus” award from the Indian Institute of Technology (IIT) Bombay in 2012, the Zinnov Award for Thought Leadership in 2014, and was elected Fellow of the Indian National Academy of Engineers in 2016.
**Panel: IC Design in The Era of Deep Learning**

**Panelist**

**Naveen Verma**  
Professor  
Princeton University

**BIO:** Naveen Verma received a B.A.Sc. degree in Electrical and Computer Engineering from the UBC, Vancouver, Canada in 2003, and the M.S. and Ph.D. degrees in Electrical Engineering from MIT in 2005 and 2009 respectively. Since July 2009 he has been at Princeton University, where he is the current Director of the Keller Center for Education in Innovation and Entrepreneurship and Professor of Electrical Engineering. His research focuses on advanced sensing systems, exploring how systems for learning, inference, and action planning can be enhanced by algorithms that exploit new sensing and computing technologies. This includes research on large-area, flexible sensors, energy-efficient statistical-computing architectures and circuits, and machine-learning and statistical-signal-processing algorithms. Professor Verma has served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society, and on the technical program committees for ISSCC, VLSI Symposia, DATE, and IEEE Signal-Processing Society (DISPS). Professor Verma is the recipient or co-recipient of the 2006 DAC/ISSCC Student Design Contest Award, 2008 ISSCC Jack Kilby Paper Award, 2012 Alfred Rheinstein Junior Faculty Award, 2013 NSF CAREER Award, 2013 Intel Early Career Award, 2013 Walter C. Johnson Prize for Teaching Excellence, 2013 VLSI Symposia. Best Student Paper Award, 2014 AFOSR Young Investigator Award, 2015 Princeton Engineering Council Excellence in Teaching Award, and 2015 IEEE Transactions CPMT Best Paper Award.

**Panelist**

**Todd Younkin**  
President and CEO  
Semiconductor Research Corporation

**BIO:** Todd Younkin is a talented and seasoned executive with more than 20 years of experience in technology innovation. Dr. Younkin’s extensive Research and Development experience spans Intel’s 0.18um to 5nm nodes with technical contributions in novel materials, nanotechnology, integration, advanced lithography, and integrated photonics. Most recently, Dr. Younkin engineered, launched, and led all programmatic aspects of the five-year, $240 million JUMP research initiative. It has six multi-university, multi-disciplinary innovation Centers with 133 faculty, 835 students, and 360 industrial engineering liaisons. It emphasizes the advancement of Computer Science, Electrical Engineering, and Materials to secure continued U.S. thought leadership.

Todd brings a wealth of expertise with strengths in areas such as cultivating relationships with strategic partners, entrepreneurship and investment strategies, technology innovation, operational excellence, and talent management. He has spent much of his career working alongside young minds that are aspiring to influence the ever-changing world of smart and autonomous electronics. He has built programs from the ground up, leveraging his entrepreneurial leadership to drive new business development that has generated multi-millions in funding. He has been a key contributor in introducing new technology advances and starting new global research in the U.S., Europe, and Asia.

Dr. Younkin holds a Ph.D. from the California Institute of Technology in Pasadena, California. He completed his Bachelor of Science at the University of Florida in Gainesville, Florida. He aspires to continue to influence the next generation of technology and inventors, bringing ideas and investors together to drive heterogeneous electronic solutions that will deliver a smarter, shared future.
Center Overview

**BIO:** Kenneth O received his S.B, S.M, and Ph.D. degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology, Cambridge, MA in 1984, 1984, and 1989, respectively. From 1989 to 1994, Dr. O worked at Analog Devices Inc. developing sub-micron CMOS processes for mixed signal applications, and high speed bipolar and BiCMOS processes. He has been a professor at the University of Florida, Gainesville from 1994 to 2009. He is currently the Director of Texas Analog Center of Excellence and TI Distinguished University Chair Professor of Analog Circuits and Systems at the University of Texas at Dallas. His research group is developing circuits and components required to implement analog and digital systems operating at frequencies up to 40 THz using silicon IC technologies. Dr. O is the President of the IEEE Solid-State Circuits Society. He has authored and co-authored ~270 journal and conference publications, as well as holding 13 patents. Dr. O has received the 2014 Semiconductor Research Association University Researcher Award. Prof. O is also an IEEE Fellow.
TxACE Analog Symposium 2020

Poster Session Proceedings

October 19, 2020
The University of Texas at Dallas
# LIST OF POSTER ABSTRACTS

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
<th>Poster #</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trim Time Reduction based on Inter-Trim Correlation</td>
<td>V. Amritur Niranjan, D. Neethirajan, C. Xanthopoulos, Y. Makris</td>
<td>1</td>
</tr>
<tr>
<td>420-GHz High Gain and Broadband Antenna</td>
<td>H. Bakshi, A. Blanchard, K. K. O.</td>
<td>2</td>
</tr>
<tr>
<td>Biomimetic Neurons for Purely Spintronic On-Chip Artificial Intelligence Applications</td>
<td>W. H. Brigner, N. Hassan, X. Hu, O. Akinola, C. Bennett, M. Marinella, F. Garcia-Sanchez, J. A. C. Incorvia, J. S. Friedman</td>
<td>3</td>
</tr>
<tr>
<td>Ultra-Low-Power Robust SAR ADC for PMCW Automotive Radar</td>
<td>Y. T. Caivin Cai, Y. Chiu</td>
<td>4</td>
</tr>
<tr>
<td>300 GHz 2nd-Order Sub-harmonic Up-conversion Mixer Using Symmetric MOS Varactors</td>
<td>Z. Chen, K. K. O.</td>
<td>5</td>
</tr>
<tr>
<td>Hardware Acceleration for Analog Circuit Analysis</td>
<td>A. Chitale, A. Pan, Y. Chiu</td>
<td>6</td>
</tr>
<tr>
<td>A high performance 2D microsupercapacitors</td>
<td>B. Dousti, Y. II. Choi, G. S. Lee</td>
<td>8</td>
</tr>
<tr>
<td>A New Active-Clamp Forward Converter with Reduced Voltage Stress and Improved Soft-Switching Performance</td>
<td>Lixiong Du, D. B. Ma</td>
<td>9</td>
</tr>
<tr>
<td>Temperature Independent Precursors for Gate Oxide Degradation Monitoring of SiC MOSFETs</td>
<td>M. Farhadi, B. Akin</td>
<td>10</td>
</tr>
</tbody>
</table>
EV Traction Drive with variable, high DC Link Voltage and 48 V Battery Pack
A. Gupta, R. Ayyanar .................................................................................................................................... 11

Stray Magnetic Flux Based Condition Monitoring Techniques for Permanent Magnet Synchronous Motors
V. Gurusamy, B. Akin .................................................................................................................................... 12

Temporal Head Pose Estimation from Point Cloud in Naturalistic Driving Conditions
S. Jha, T. Hu, C. Busso .................................................................................................................................... 13

Package, Transmission Line Design and Characterization for Antenna in Package Solutions
A. Jogalekar, M. Iyer, R. Henderson ............................................................................................................. 14

A 10-Output Single-Inductor-Multiple-Output DC-DC Buck Converter with 200-pF Integrated Output Capacitors for a Sub-mW Multi-Voltage Domain System-on-Chip
D. Kim, S. J. Kim, Z. Jiang, S. Kim, A. Blanco, R. K. Krishnamurthy, M. Seok ............................................. 15

Power Loss Analysis on 48V-to-1V Single Stage Switched-Mode Power Converters
J. W. Kwak, D. B. Ma .................................................................................................................................... 16

Load Modulated Balanced mm-wave CMOS PA with Integrated Linearity Enhancement for 5G Applications
Z. Liu, C. Chappidi, T. Sharma, K. Sengupta ................................................................................................ 17

High Frequency Dielectric Characterization of Substrates Using a Single Air Line
N. Mahjabeen, R. Henderson ........................................................................................................................ 18

A New Deep Learning Approach for Statistical Gaze Regions Estimation in Naturalistic Driving Environments
M. Marzban, S. Jha, C. Busso, N. Al-Dhahir ................................................................................................. 19

Millimeter-wave Broadband Antennas in Package (AiP) and Interconnects for Industrial Systems
O. Medina, R. Henderson, M. Iyer .............................................................................................................. 20

Dominant Failure sites and probable failure modes in GaN HEMTS under static gate stressing
A. Mehta, S. Shichijo, M. Kim ........................................................................................................................ 21
<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Machine Learning-based Impairments Classification and Decomposition in RF Transceivers</td>
<td>D. Neethirajan, C. Xanthopoulos, K. Subramani, K. Schaub, I. Leventhal, Y. Makris</td>
<td>23</td>
</tr>
<tr>
<td>Developing Lifetime Estimation Toolbox for SiC MOSFET Considering System Mission Profile</td>
<td>S. Pu, B. Akin</td>
<td>24</td>
</tr>
<tr>
<td>3-D Holographic Near-Field MIMO-ISAR Millimeter-Wave Imaging</td>
<td>J. Smith, M. Torlak</td>
<td>26</td>
</tr>
<tr>
<td>Design of Folded Reflectarray Antenna (FRA) for 0.41 THz Imaging</td>
<td>N. Virushabadoss, R. Henderson</td>
<td>28</td>
</tr>
<tr>
<td>Performance Degradation of Power MOSFETs under Repetitive Avalanche Breakdown Test</td>
<td>C. Xu, B. Akin</td>
<td>30</td>
</tr>
<tr>
<td>Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching</td>
<td>P. Zhou, J. A. Smith, L. Deremo, S. K. Heinrich-Barna, J. S. Friedman</td>
<td>31</td>
</tr>
<tr>
<td>Terahertz Active Imaging Radar with 2-D Scalable Concurrent Transceiver Pixels in 65-nm CMOS</td>
<td>Yukun Zhu, P. R. Byreddy, K. K. O, W. Choi</td>
<td>32</td>
</tr>
</tbody>
</table>
Trim Time Reduction based on Inter-Trim Correlation

V. Amritur Niranjan, D. Neethirajan, C. Xanthopoulos, Y. Makris

Email: vxa172230@utdallas.edu

Abstract 1- To curb the impact of process variation on manufactured ICs and their performance parameters, the IC is subjected to the process of trimming. During the process of trimming there is a need to search the trim code space extensively. The trim code search is crucial in identifying a trim code that results in the IC’s performance parameter measuring in the specification region. This search to identify the appropriate trim code increase with increasing IC’s complexity and number of components to be trimmed on the IC. This Increases the overall trim time. In order to alleviate this we propose a machine learning based approach that takes advantage of the correlation between different trims to identify the optimal trim code.
420-GHz High Gain and Broadband Antenna

H. Bakshi, A. Blanchard, K. K. O

Email: hxb160030@utdallas.edu

Abstract 2- The aim of this work is to design a 420-GHz high gain and broadband on-chip antenna using a 65-nm CMOS foundry process which has 10 copper layers and one aluminum layer. A series-fed patch antenna comprising of eight rectangular patch elements is designed on the aluminum bond pad layer with its ground on metal 6. A ground wall surrounding the antenna is constructed by shunting metals 6-10. The antenna is encapsulated in a Quad-Flat No-Leads (QFN) package made of materials based on silica microparticles dispersed in an epoxy matrix, which is shown to improve the antenna performance. The packaged antenna results in 160-GHz of -10 dB $|S_{11}|$ bandwidth, 9-dB Gain and 45% radiation efficiency at 420 GHz.
Biomimetic Neurons for Purely Spintronic On-Chip Artificial Intelligence Applications

W. H. Brigner, N. Hassan, X. Hu, O. Akinola, C. Bennett, M. Marinella, F. Garcia-Sanchez, J. A. C. Incorvia, J. S. Friedman

Email: Wesley.Brigner@utdallas.edu

Abstract 3- Due to their volatile and binary nature, the complementary metal-oxide-semiconductor (CMOS) transistor technology used in standard von Neumann computer architectures are ideal for processing structured information, but are inadequate when attempting to process unstructured, real-world data. To resolve this issue, novel architectures are being designed that attempt to mimic the human brain. These biomimetic neuromorphic architectures typically contain two separate device types – neurons and synapses. Although a plethora of novel beyond-CMOS devices, including other semiconductor devices, designed to implement these functions already exist, they still are highly dependent on CMOS technology to provide control signals, cascadability, and secondary system-level functions. In turn, this additional circuitry vastly increases the power consumption and fabrication complexity of the systems they are incorporated in. Magnetic domain wall (DW) based spintronic devices, on the other hand, show promise to intrinsically implement biomimetic functions without requiring control circuitry – even so, previous proposals using these devices still use CMOS for the very same purpose. To resolve this issue, we propose three new spintronic neurons capable of intrinsically implementing vital neuronal and synaptic functions without any external circuitry.
Ultra-Low-Power Robust SAR ADC for PMCW Automotive Radar

Y.T. Caivin Cai, Y. Chiu

Email: ycc160030@utdallas.edu

Abstract 4- Phase-modulated continuous-wave (PMCW) radar applications require novel analog techniques to address the digital intensive architecture that is suitable for CMOS implementations. CMOS SAR ADCs are suitable to address the specs of a low-power, high-sample rate ADC for PMCW radar; however, certain concerns arise when considering the poor BER performance and power consumption of the total system including the peripheral components of the SAR ADC. To achieve low power consumption and a significant BER reduction, three techniques are proposed: “elastic” S/H, a pre-charging technique for minimum charging and discharging of the DACs, and the split-ADC architecture. The first technique, called “elastic” S/H, allows distortion that is canceled out by the sampling capacitor and DAC capacitor during the quantization process. Elastic S/H saves power in the ADC input driver by allowing a larger swing compared to conventional designs, and the S/H linearity is maintained due a bootstrapped input switch. The second technique greatly saves power on reference drivers by pre-charging the DAC capacitors with a constant reference charge. The final technique of utilizing a split-ADC architecture comes at a negligible SNR penalty and should enhance the BER of the SAR ADC to $p^2$, where $p$ is the raw BER of a single SAR. The proposed approach of elastic S/H, minimum charging and discharging of the DAC, and split-ADC architecture allows for a low-power robust SAR ADC.
300 GHz 2\textsuperscript{nd}-Order Sub-harmonic Up-conversion Mixer Using Symmetric MOS Varactors

Z. Chen, K.K.O

Email: zxc121030@utdallas.edu

Abstract 5- A 2nd-order sub-harmonic up-conversion mixer with IF of 150 GHz and RF of 290 GHz that employs accumulation mode MOS symmetric varactors is demonstrated in 65-nm CMOS. A transformer-based hybrid is utilized to improve port isolation. The mixer achieves the maximum conversion gain of -16 dB including the losses (~2 dB total) of input and output baluns added for measurements. The LO power at 70 GHz is 11.5 dBm and the 27-GHz 3-dB bandwidth spans between 284 and 311 GHz. The -11.6 dBm output 1-dB compression point from a single mixer is the highest among that for the 2nd-order sub-harmonic mixers with RF of ~300 GHz fabricated in any process technologies. The proposed mixer suggests that up-conversion mixers using varactors in CMOS operating near 300 GHz can have superior performance for frequency up-conversion and a better power handling capability.
Hardware Acceleration for Analog Circuit Analysis

A. Chitale, A. Pan, Y. Chiu

Email: aac141430@utdallas.edu

Abstract - Circuit simulation is needed to verify the functionality of analog circuits. However, simulations executing on a single processing thread may take too long to complete, especially if many simulations need to be performed or if the circuit has a long settling time. Additional hardware such as GPUs and FPGAs, respectively, can greatly accelerate those simulations. For fully parallelizable tasks such as parametric sweeps or Monte Carlo simulations, simply adding more processor cores can also result in a significant speedup.
A Wideband 180-GHz MSK Transceiver for Dielectric Waveguide Communication

Email: Shenggang.Dong@utdallas.edu

Abstract 7- High data rate 180-GHz MSK modulated signals for dielectric waveguide communication with an output power of -3.5dBm are demonstrated using a signal generator fabricated in 65-nm CMOS. To accomplish this, techniques for controlling the relative phases of half-sine shaping signal and data, “Misaligned-to-Aligned” are proposed and demonstrated. Limited by the instrumentation for MSK signal analyses, the eyes of transmitted MSK signals have been verified for a data rate up to 10 Gbps. The spectra of transmitted signals for data rate up to 15 Gbps are also demonstrated. The MSK signal generator provides 5X higher data rate among all the previously reported MSK transmitters at 3X higher carrier frequency.

A 180 GHz mixer-first phase-locked-loop based MSK receiver is demonstrated in 65-nm CMOS. Double balanced anti-parallel-diode-pair (APDP) based sub-harmonic mixer forms the phase detector. Compensation using multiple zeros reduces the effect of in-loop delay on the stability of PLL. Without external LO synchronization, the receiver achieves 10 Gbps with a BER < 10^{-12} at -24-dBm available input power. The open loop measurements show the down-conversion chain has a 3-dB bandwidth of approximately 48 GHz at 180 GHz and the minimum single side band (SSB) noise figure of 18.6 dB. This receiver is the self-synchronized receiver using coherent detection with the highest operating frequency in CMOS when published. This work also demonstrates that a PLL based receiver can support data rates in excess of 10 Gbps.
A high performance 2D microsupercapacitors

B. Dousti, Y. Il. Choi, G. S. Lee

Email: Behnoush.dousti@utdallas.edu

Abstract 8- 2D microsupercapacitors (MSCs) has shown a great promise as microscale power source for on-chip application where the footprint area of the device matters the most. Current miniaturization trend demands for smaller power sources with higher energy density. New approaches are being investigated to improve the energy density of the thin film MSCs through employing novel materials and viable designs. Highly aligned carbon nanotubes (HACNT sheets) have recently attracted great attention in developing high-performing ultrathin supercapacitors which take advantage of the long-range alignment to improve electrochemical performance. Here, we took advantage of this novel material to fabricate our microsupercapacitors. Our ultrathin MSC devices demonstrate high specific capacitance of 80 F/cm³ and energy density (~20 mWh/cm³) comparable to thin film lithium batteries. Current findings confirm the potential of HACNT for future 2D high energy density microsupercapacitors.
A New Active-Clamp Forward Converter with Reduced Voltage Stress and Improved Soft-Switching Performance

Lixiong Du, D. Brian Ma

Email: lixiong.du@utdallas.edu

Abstract 9- The 48V power delivery architecture has been applied to replace the 12V approach in datacenters, reducing the power distribution loss by 16 times to support higher current. To achieve high power density and efficiency, direct DC-DC conversion from 48V down to 1V is highly desirable to power the point of load. Such high step-down conversion ratio makes it challenging if using conventional buck converters due to the extremely short on-duty time. Hybrid converters can realize the duty-cycle extension and operate at higher switching frequency. However, they require a large amount of circuit components for multi-phase operation, increasing the bill of materials (BOM) cost and design complexity. Isolated converters provide great flexibility to accomplish high step-down conversion due to the transformer turns ratio. Among the isolated converter topologies, active-clamp forward (ACF) converter becomes attractive as it has the simple structure and doesn’t have the voltage spike. But the primary switches in ACF converter suffer from high voltage stress. Here we present a buck-assisted ACF converter to mitigate this challenge. By building the buck-assisted input stage and active-clamp stage separately, the maximum voltage stress is reduced by 25% for 48V-to-1V conversion. Devices with low-voltage ratings are employed to reduce the parasitic capacitance. Therefore, a smaller leakage inductor is capable of zero-voltage switching (ZVS). And the current commutation speed in the secondary side is improved, decreasing its turn-off loss greatly.
Temperature Independent Precursors for Gate Oxide Degradation Monitoring of SiC MOSFETs

M. Farhadi, B. Akin

Email: Masoud.Farhadi@UTDallas.edu

Abstract 10- Gate oxide degradation has triggered a big challenge in the reliability of SiC MOSFETs and show the necessity of the development of new condition monitoring systems to meet the future application trends and customer expectations. Various precursors have been introduced in the literature for gate oxide degradation monitoring. However, there is no junction temperature independent precursor for gate oxide degradation so far. In this paper, two new precursors (miller capacitance and gate-source capacitance) with junction temperature independent feature for gate oxide degradation monitoring of SiC MOSFETs are proposed. Gate oxide degradation mechanism and its effect on junction capacitances is analyzed in depth. During the accelerated aging tests (with high electric field and high temperature), consistent change of miller capacitance and gate-source capacitance is confirmed for both common source and kelvin source SiC MOSFETs. Also, temperature sensitivity of each precursors is investigated. An early warning in–situ circuit to detect aging based on variations in these precursors is proposed. Also, a comparison with currently available precursors is given to show the merits of the proposed precursors. Finally, the experimental results are presented to verify the validity of the theoretical analysis and distinguish ability of the proposed circuit.
EV Traction Drive with variable, high DC Link Voltage and 48 V Battery Pack

A. Gupta, R. Ayyanar

Email: agupt164@asu.edu

Abstract 11- In EV traction systems, higher voltage motors offer improved efficiency and power density. However, the optimum battery voltage is low considering factors such as issues with large number of cells in series and safety. In order to individually optimize the motor and battery voltages, a DC-DC converter between the battery and inverter stage has been implemented in recent production hybrid electric vehicles. The DC link is controlled to be variable, following the motor speed. With this architecture, the battery voltage is still 200V to 400V for most commercial vehicles. Typically, a boost DC-DC converter is employed, and hence, the DC link cannot go below the battery voltage, limiting the benefits of the DC-DC converter. During emergencies, the highest voltage present even with all converters turned off is the battery voltage in the range of 400 V. The proposed architecture with multiple 48 V battery stacks and multi-input high conversion ratio DC-DC converters, can reduce the maximum voltage in the vehicle during emergencies to 48V, mitigate issues with large number of cells in series, eliminate the need for a separate auxiliary power DC-DC converter, and extend the benefit of variable DC link over a larger speed range. The multi-input high conversion ratio DC-DC converter provides an added advantage of using lower voltage stress devices thus, improving the efficiency and cost effectiveness of the solution.
Stray Magnetic Flux Based Condition Monitoring Techniques for Permanent Magnet Synchronous Motors

V. Gurusamy, B. Akin

Email: Vigneshwaran.Gurusamy@utdallas.edu

Abstract 12- Permanent magnet (PM) motor market is growing significantly due to its high energy efficiency and power density. The widespread deployment requires condition monitoring techniques to ensure the reliability. Stray magnetic field is the externally radiated magnetic field around the motor which provides detailed information about the health condition of motor. We have developed different techniques to detect and locate various faults in PM motors based on sensing the stray magnetic flux around the motor through TI’s fluxgate sensor. Here we present our methods to detect two most common faults in electrical motors, bearing fault and inter-turn short circuit fault and a technique to estimate temperature of permanent magnets in the motor. The developed techniques are very practical and is superior to existing techniques based on motor current sensing. The proposed methods are verified with 2D- Finite element simulations and validated with extensive experiments.
Temporal Head Pose Estimation from Point Cloud in Naturalistic Driving Conditions

S. Jha, T. Hu, C. Busso

Email: sumit.jha@utdallas.edu

Abstract 13 - Head pose estimation is an important problem as it facilitates tasks such as gaze estimation and attention modeling. In the automotive context, head pose provides crucial information about the driver's mental state, including drowsiness, distraction and attention. It can also be used for interaction with in-vehicle infotainment systems. While computer vision algorithms using regular cameras are reliable in controlled environments, head pose estimation is a challenging problem in the car due to sudden illumination changes, occlusions and large head rotations that are common in a vehicle. These issues can be partially alleviated by using depth cameras. Head rotation trajectories are continuous with important temporal dependencies. Our study leverages this observation, proposing a novel temporal deep learning model for head pose estimation from point cloud. The approach extracts discriminative feature representation directly from point cloud data, leveraging the 3D spatial structure of the face. The frame-based representations are then combined with bidirectional long short term memory (BLSTM) layers. We train this model on the newly collected multimodal driver monitoring (MDM) dataset, achieving better results compared to non-temporal algorithms using point cloud data, and state-of-the-art models using RGB images. We further show quantitatively and qualitatively that incorporating temporal information provides large improvement not only in accuracy, but also in the smoothness of the predictions. We also analyze the effect of the number of temporal layers in the model.
Package, Transmission Line Design and Characterization for Antenna in Package Solutions

A. Jogalekar, M. Iyer, R. Henderson

Email: anj170004@utdallas.edu

Abstract 14- Front-end module (FEM) integration and packaging have been identified as a key research challenge for millimeter (mm) wave communications. Antenna in Package (AiP) is a key research element enabling the realization of future mm-wave FEMs. This research focuses on development of AiP technologies on multiple packaging types such as QFN, Routable Lead Frame, Fanout WCSPs and substrate-based packages. The package models, suitable transmission lines and antenna types that go with the above mentioned package types will be designed and simulated initially for their performance in the frequency bands of 90-220GHz. Two packages are expected to be shortlisted at the end of the first nine months of the project. Test vehicles and package prototypes will be built, and high frequency measurements will be performed on these package prototypes. The simulated and measured data will be compared, and design guidelines/recommendations will be given for suitable antenna in package structures to operate in the frequency bands 90-220GHz.
A 10-Output Single-Inductor-Multiple-Output DC-DC Buck Converter with 200-pF Integrated Output Capacitors for a Sub-mW Multi-Voltage Domain System-on-Chip

D. Kim, S. J. Kim, Z. Jiang, S. Kim, A. Blanco, R. K. Krishnamurthy, M. Seok

Email: dk2990@columbia.edu

Abstract 15- Emerging sub-mW near-threshold-voltage system-on-chips require new power management architecture that can create multiple voltage domains with the fewest possible off-chip passives. To fulfill this need, we propose an ultra-low-power single-inductor-multiple-output (SIMO) DC-DC buck converter in a 65 nm CMOS process technology. Featuring hybrid time- and event-driven digital control for ultra-low feedback latency, this DC-DC converter takes 1-V input voltage and produces ten independent output voltages from 0.4 to 0.8 V at the aggregated power delivery of 0.465 mW. It has ten 200-pF on-chip output capacitors and one 82-μH off-chip inductor and achieves the peak power conversion efficiency of 80.8% while the ripple size is less than 10% of each output voltage.
Power Loss Analysis on 48V-to-1V Single Stage Switched-Mode Power Converters

J. W. Kwak, D. B. Ma

Email: jinwoong.kwak@utdallas.edu

Abstract 16: Along with the exponential growth of datacenter business, power delivery systems for datacenters act quickly to adopt 48V power architecture in order to achieve less distribution (I2R) loss, higher power density, and reduced cost. However, 48V power architecture faces major challenge in its efficiency of direct power conversion from 48V down to 1V. This poster presents a comparative power loss analysis between half-bridge buck converter, multi-level buck converters, and hybrid Dickson converters. The performance of each converter was verified in a high voltage 0.18μm BCD process, with major power switches implemented with power LDMOS FETs. The switch sizes of each converter were optimized at load current of 10A and effective output switching frequency (fSW,EFF) of 1MHz. Inductor sizes were selected to keep current ripples at 1.5A, while flying capacitor sizes were selected to keep voltage ripples within 5% of respective capacitor voltages. Output capacitors were selected to keep the output ripples below 10mV. In the load range from 1A to 30A, multi-level buck converters achieve at least 12% higher efficiency than half-bridge buck converter but with at least 92% silicon area overhead. Hybrid Dickson converters achieve at least 19.2% higher efficiency than half-bridge buck converter, and a double series-capacitor buck converter achieves over 90% efficiency at 10A while keeping silicon area overhead within 38%.
Load Modulated Balanced mm-wave CMOS PA with Integrated Linearity Enhancement for 5G Applications

Z. Liu, C. Chappidi, T. Sharma, K. Sengupta

Email: zhengl@princeton.edu

Abstract 17- The opening of the disjointed bands from 28 GHz and beyond for 5G applications creates a need for multi-band reconfigurable front-ends where simultaneously broadband and back-off efficient power amplifiers remain one of the critically challenging blocks. This is particularly difficult at mm-wave frequencies, where PA output power, peak and back-off efficiency and bandwidth trade off strongly against each other. In this aspect, load modulated balanced amplifier has been proposed recently at RF exploiting a broadband balanced amplifier architecture and exploiting the isolated port as a load modulation port. Till date only low frequent RF PAs using packaged transistors and off the shelf components have been demonstrated.

The paper presents the first mm-Wave load modulated balanced amplifier (LMBA) architecture across 30-40 GHz. The architecture is implemented with a transformer-based hybrid at input and output to allow wideband power combining and achieve high isolation with a control PA for load-modulation and back-off efficiency enhancement across 30-40 GHz. To overcome the compressive behavior of an LMBA and enhance linearity, an integrated adaptive biasing is integrated on-chip allowing superior ACLR performance across 30-40 GHz. Under CW excitation, the two-stage LMBA demonstrates output power of 18.5-20 dBm, output drain efficiency >30% across 30-40 GHz. The modulation capabilities of LMBA are tested using a 64 QAM signal with a data rate of 6Gbps wherein PA demonstrates EVM of -26.4 dB and ACLR of -29 dBC at an average output power of 10.6 dBm. To the best of the authors’ knowledge, this is the first load-modulated balanced PA at mm-wave in silicon.
High Frequency Dielectric Characterization of Substrates Using a Single Air Line

N. Mahjabeen, R. Henderson
Email: nxm152530@utdallas.edu

Abstract 18- Dielectric properties of substrates are crucial in the microwave regime to design circuits. A key requirement is to have reliable dielectric constant and loss tangent values over a wide bandwidth at high frequency. Many substrate manufacturers like Rogers and Isola provide the properties at 10 GHz using industry standard IPC TM 650 2.5.5.5, which is a resonant characterization technique. They also provide properties from 8 GHz to 40 GHz using a non-resonant characterization technique. To design high frequency circuits, the knowledge of dielectric properties extending beyond 40 GHz is of growing importance. This poster presents a method to extract wideband dielectric properties, for the first time up to 67 GHz, using a single coaxial transmission line. The algorithm used to extract the properties is Chalapat’s reference-plane-invariant (RPI) which combines Nicolson-Ross-Weir and Baker-Jarvis methods. The algorithm recommends the material sample length to be less than 0.5λ to avoid Fabry-Perot resonance. This reduces the measurement sensitivity and uncertainty in the results. To improve this, we have introduced stacking of fixed thickness samples to increase the total length of the material under test (MUT). A cost-effective solution calibration method is used and the dielectric properties of RT/duroid® 5880 have been studied using a 1.85 mm air line for the first time.
A New Deep Learning Approach for Statistical Gaze Regions Estimation in Naturalistic Driving Environments

M. Marzban, S. Jha, C. Busso, N. Al-Dhahir

Email: mohamed.marzban@utdallas.edu

Abstract 19- Precise gaze estimation in naturalistic driving environments without occluding the feature space is considered a major research challenge. Our goal is to exploit data from different in-vehicle sensors to monitor and assess the visual attention of the driver, producing statistical estimates for the driver’s elevation and azimuth gaze angles. The proposed gaze detection algorithms can help in evaluating and analyzing driver distractions, and producing valuable information to alarm the driver in case of distraction. In addition, they can play a key role in deciding whether to hand control to a human operator in level 3 and 4 autonomous vehicles. We start by utilizing AprilTags to estimate the precise location of the driver’s gaze during driving. Then, we collect new continuous gaze data, while the car is parked, that spans all possible in-vehicle azimuth and elevation gaze angles and augment it to the driving gaze data. We detect the face and the eyes of the drivers to observe subtle gaze feature and feed them to our developed deep learning architecture that outputs statistical estimates for each gaze angle. We utilize random search to optimize and tune the model hyper-parameters. We produce a high-accuracy and high-precision probabilistic elevation and azimuth angles estimates on new drivers that the network has never seen before which demonstrates the generalization capabilities of our gaze estimation algorithm.
Millimeter-wave Broadband Antennas in Package (AiP) and Interconnects for Industrial Systems

O. Medina, R. Henderson, M. Iyer
Email: oxm161130@utdallas.edu

**Abstract** - The integration of antennas in package (AiP) has become more plausible since newer millimeter-wave integrated circuits keep shrinking in size and leaving space available to place these antennas within the package. Typically, these integrated circuits are encapsulated using mold compounds that provide mechanical stability and protection from the outside world. It is a necessity for mold compounds to have good RF characteristics throughout the circuit’s operating bandwidth if we are to realize an AiP. This poster presents the design of antennas that operate in the WR8 band (90GHz-140GHz) and WR5 band (140GHz-220GHz). In the end, the selection of the best fitting antenna will depend on the type of package and performance required by the specific industrial application.
Abstract 21- GaN HEMTs are promising candidates in the modern-day power application sector, and based on the mode of static stressing, the impact of the onset of failure in a device is different. It can strongly influence the device’s lifetime. The present study is an effort to understand the transition from soft breakdown to the hard breakdown in AlGaN/GaN layered E-mode GaN HEMTS devices during static stressing. The important variables are constant voltage and constant current stressing on the p-GaN gate; temperature also plays a vital part in the devices’ operation and stability. Devices were stressed at constant gate voltage and constant current (cc) at different temperatures till breakdown. Similar devices showed different breakdown, devices under cc showed softer breakdown compared to devices failing catastrophically under constant voltage stress. Devices at higher temperature showed considerably more stable operation and consistent lifetimes. Furthermore, devices under constant current showed better stability compared to devices stressed under constant voltage. Soft (SDB) or Hard dielectric breakdown (HDB) has a lot to do with failure’s morphology. HDB usually is accompanied by visible damage on gate contacts, gate fingers and at AlGaN/GaN interface, while SDB can be due to a percolation path formation. AlGaN/GaN heterostructure is damaged, which can support the percolation path theory. Failed devices have been de-capped and studied under an electron microscope for observing the areas of failure.
315-GHz CMOS Minimum Shift Keying Transceiver

I. Momson, S. Dong, P. Yelleswarapu, Z. Chen, W. Choi, K. K. O

Email: ibukun.momson@utdallas.edu

Abstract - The increasing $f_r/f_{max}$ of silicon integrated circuits technology has enabled generation of carrier signals in the millimeter and sub-millimeter wave frequencies where the narrow fractional bandwidth of carriers translates to large absolute coherence bandwidths. These high frequency carriers and the associated wide coherence bandwidths make possible high data rate wireless and dielectric waveguide short range communications. By multiplexing a carrier band among a set of sub-millimeter wave carrier bands (frequency division multiplexing), it should be possible to use this portion of the spectrum to support data rates approaching that of optical communication systems without requiring the use of photonic components. This work presents a 315-GHz minimum shift keying (MSK) transceiver used to form an on-chip link that supports a data rate of up to 10 Gbps with a BER $< 10^{-11}$ at -21-dBm receiver sensitivity. The transmitter generates up to -11 dBm of single tone power at 315 GHz. The receiver is a phase-locked loop (PLL) based design that demodulates MSK signals and includes a 1-bit analog-to-digital converter (ADC) to generate a digital bit stream output. The link does not require separate frequency synchronization between the transmitter and receiver because the receiver operation tracks the carrier frequency of the transmitted signal. This work demonstrates that a PLL based self-synchronized coherent detection can be made to work at 300 GHz in a CMOS process with an $f_{max}$ of ~300 GHz, while supporting a data rate of 10 Gbps.
Machine Learning-based Impairments Classification and Decomposition in RF Transceivers

D. Neethirajan, C. Xanthopoulos, K. Subramani, K. Schaub, I. Leventhal, Y. Makris

Email: deepika.neethirajan@utdallas.edu

Abstract: We propose a machine learning-based solution for noise classification and decomposition in RF transceivers. Wireless transmitters are affected by various noise sources, each of which has a distinct impact on the signal constellation points. The proposed approach takes advantage of the characteristic dispersion of points in the constellation by extracting key statistical and geometric features that are used to train a machine learning model. The trained model is, then, capable of identifying the noise source fingerprint, comprised by single or multiple noise sources, for each affected device. Effectiveness of the model has been verified using constellation measurements from a combined set of simulated and actual silicon devices.
Abstract 24- In this study, a toolbox developed for predicting SiC MOSFET consumable lifetime in field application is presented. Through system mission profile and converter model, the power dissipation on device under study is calculated by device electrical model. In order to enhance the estimation accuracy, automated curve tracer and double pulse tester is used to generate mapping between junction temperature, bus voltage, load current and power loss. A electro-thermal model is established in Matlab/Simulink to derive device’s junction temperature profile. A Rainflow counting algorithm is used to transfer time domain junction temperature profile into thermal mechanical stress cycles and accumulated damage during each mission profile is calculated. A full bridge DC-DC converter is used to illustrate the lifetime predicting process of developed toolbox.
Radar Musical Instrument – A Spatiotemporal Real-Time mmWave Sensor for Contactless Human-Computer Interaction

J. Smith, M. Torlak
Email: jws160130@utdallas.edu

Abstract 25- Millimeter-wave (mmWave) radar sensing is transforming many applications that have traditionally required different modes of sensing, as exemplified by self-driving cars, vital signs monitoring, fall detection, occupancy detection, and many more. Human-computer interaction can benefit from the use of mmWave radars thanks to the fine depth and cross-range resolution of such devices enabling accurate tracking of user-performed actions in space. Additionally, radar modulation schemes with multiple transmit and receive antennas, such as frequency-modulated continuous-wave (FMCW), can produce return signals containing accurate information describing the motion of targets in space and time. Spatiotemporal algorithms can be employed to extract useful features of hand gestures performed by a user from the rich radar return data. In this paper, we propose and demonstrate a novel real-time mmWave sensor that leverages spatiotemporal information from a multiple-input-multiple-output (MIMO)-FMCW radar to create a new musical interface (NMI) controllable by specific hand positions and motions performed by the musician. After constructing the necessary real-time framework, a simple signal processing chain and feature extraction method is presented and subsequently extended to an enhanced tracking technique employing novel localization algorithms and deep-learning-based spatiotemporal enhancement. The novel system we propose in this paper allows for real-time human-computer interaction to create a new musical interface controlled solely by the precise tracking of the musician's hand.
3-D Holographic Near-Field MIMO-ISAR Millimeter-Wave Imaging

J. Smith, M. Torlak
Email: jws160130@utdallas.edu

Abstract - Multiple-input-multiple-output (MIMO) millimeter-wave (mmWave) sensors for synthetic aperture radar (SAR) and inverse SAR (ISAR) address the fundamental challenges of cost-effectiveness and scalability inherent to near-field imaging. In this paper, near-field MIMO-ISAR mmWave imaging systems are discussed and developed. The rotational ISAR (R-ISAR) regime investigated in this paper requires rotating the target at a constant radial distance from the transceiver and scanning the transceiver along a vertical track. Using a 77GHz mmWave radar, a high resolution three-dimensional (3-D) image can be reconstructed from this two-dimensional scanning taking into account the spherical near-field wavefront. While prior work in literature consists of single-input-single-output circular synthetic aperture radar (SISO-CSAR) algorithms or computationally sluggish MIMO-CSAR image reconstruction algorithms, this paper proposes a novel algorithm for efficient MIMO 3-D holographic imaging and details the design of a MIMO R-ISAR imaging system. The proposed algorithm applies a multistatic-to-monostatic phase compensation to the R-ISAR regime allowing for use of highly efficient monostatic algorithms. We demonstrate the algorithm’s performance in real-world imaging scenarios on a prototyped MIMO R-ISAR platform. Our fully integrated system, consisting of an mechanical scanner and efficient imaging algorithm, is capable of pairing the scanning efficiency of the MIMO regime with the computational efficiency of single pixel image reconstruction algorithms.
A Survey of Feature Extraction Methods for Machine Learning-Based Hotspot Detection

S. Tellakula, G. R. Reddy, Y. Makris

Email: suraag.tellakula@utdallas.edu

Abstract 27: Design patterns from sub-wavelength technology nodes may not be reliably printed on silicon even though they are Design Rule Check (DRC) clean and comply with Design For Manufacturability Guidelines (DFMGs). Such patterns are known as weak-points/hotspots and there is an imminent need to identify and fix them well-before fabrication. Since their inception, several hotspot detection solutions have been proposed, each of them with a premise of having better accuracy, lower false alarm rates or faster training times. As a part of such hotspot detection flows, the community has also proposed several novel feature extraction techniques customized for this application. In this work, we focus mainly on feature extraction techniques and survey all such methods, and also perform an experimental comparison between them to clearly understand the impact and importance of feature extraction in hotspot detection applications.
Design of Folded Reflectarray Antenna (FRA) for 0.41 THz Imaging

N. Virushabadoss, R. Henderson

Email: nxv130230@utdallas.edu

Abstract 28- Terahertz imaging is an emerging non-destructive evaluation (NDE) technique used for material analysis and quality control. In order to perform the material analysis, the imaging system needs to have a very high directive antenna. In this poster we will present progress towards the design of a high directive antenna that will be used for a 0.41 THz CMOS imaging system. The gain specification based on the link budget analysis is 47dB. Parabolic antennas typically have a very high directionality, but the accuracy depends on curve finesse especially which is particularly critical in the THz range. The complexity of the structure can be reduced by using a planar reflectarray antenna which mimics the parabolic antenna. The reflectarray antenna is illuminated by a source which is at the boresight of the reflectarray and the gain of the reflectarray antenna is reduced significantly because of the feed blockage. A folded reflectarray antenna (FRA) is a technique in which the feed blockage can be avoided. In addition to the regular reflectarray antenna the FRA uses a grid polarizer which is also a planar structure just like the reflectarray. This poster will discuss the theory and implementation of a low-frequency scaled FRA designed using HFSS.
Always-On, Sub-300-nW, Event-Driven Spiking Neural Network based on Spike-Driven Clock-Generation and Clock- and Power-Gating for an Ultra-Low-Power Intelligence Device


Email: dw2773@columbia.edu

Abstract - Always-on artificial intelligent (AI) functions such as keyword spotting (KWS) and visual wake-up tend to dominate total power consumption in ultra-low power devices. A key observation is that the signals to an always-on function are sparse in time, which a spiking neural network (SNN) classifier can leverage for power savings, because the switching activity and power consumption of SNNs tend to scale with spike rate. Toward this goal, we present a novel SNN classifier architecture utilizing spike-driven clock-generation, clock-gating, and power-gating for a low-power design of always-on functions. The prototype is fabricated in 65nm CMOS and demonstrates sub-300nW power consumption at the competitive inference accuracy for a KWS and other always-on classification workloads.
Performance Degradation of Power MOSFETs under Repetitive Avalanche Breakdown Test

C. Xu, B. Akin

Email: cxx150130@utdallas.edu

Abstract 30- Avalanche ruggedness is one of the key factors for safe and reliable power converters deployed in various automotive subsystems. In this post, the avalanche capability of Power MOSFETs is tested under different repetitive avalanche conditions to differentiate the die degradation and package degradation. While examining the degradation mechanisms, the corresponding electrical parameter shifts are analyzed to better understand the structural changes, root causes, and identify potential precursors for condition monitoring. For this purpose, a high resolution and cost-effective nano-second Current Pulse Generator (CPG) is designed. Thanks to the high resolution PWM function of a digital signal processor (DSP), short current pulses can be generated in the order of 100 picoseconds where the magnitude and duration of the current pulse width can be adjusted precisely. During the experiments, power MOSFETs are stressed under two different pulse widths. It is observed that the on-state resistance gradually increases in both cases yet the roots of the degradations are different. The die degradation and package degradation are responsible for the changes in short pulse and long pulse, respectively. In short pulse case, some devices show saturation in drain leakage current and on-state resistance, while some others show a significant threshold voltage drop, which leads to a noticeable shift of transfer and output characteristics. The electrical parameter shifts indicate a possible gate degradation after the device aging. At the end of the tests, failure analyses are conducted on both devices under test (DUTs) under different stress conditions, revealing different failure mechanisms.
Synchronous Unsupervised STDP Learning with Stochastic STT-MRAM Switching

P. Zhou, J. A. Smith, L. Deremo, S. K. Heinrich-Barna, J. S. Friedman

Email: peng.zhou@utdallas.edu

Abstract 31- The use of analog resistance states for storing weights in neuromorphic systems is impeded by fabrication imprecision and device stochasticity that limit the precision of synapse weights. This challenge can be resolved by emulating analog behavior with the stochastic switching of the binary states of spin-transfer torque magnetoresistive random-access memory (STT-MRAM). However, previous approaches based on STT-MRAM operate in an asynchronous manner that is difficult to implement experimentally. This presentation proposes a synchronous spiking neural network system with clocked circuits that perform unsupervised learning leveraging the stochastic switching of STT-MRAM. The proposed system enables a single-layer network to achieve 100% inference accuracy on the 7x7 dataset.
Terahertz Active Imaging Radar with 2-D Scalable Concurrent Transceiver Pixels in 65-nm CMOS

Yukun Zhu, P. R. Byreddy, K. K. O, W. Choi

Email: yxz173830@utdallas.edu

Abstract 32- A novel terahertz imaging radar based on focal plan array is proposed. To incorporate the reflective mode imaging and the large-scale array for wide field of view, each pixel must include the on-chip antenna, transmitter, receiver and LO generation for coherent detection. Besides, a Cassegrain reflector can be used to extend the operating range of the imaging radar. With 65-nm CMOS process, two concurrent transceiver pixels at 300-GHz and 426-GHz have been implemented. Take the 426 GHz pixel as an example, a link margin of 12 dB is expected for reflection-mode imaging of an object with a radar cross section of ~100 cm² at 5 m away. In addition, the terahertz imagers can be packaged with costless process, like QFN. The proposed imaging radar paved a new path for the future affordable terahertz imaging system with a better sensitivity and high resolution.